Ultra-Low-Energy Three-Dimensional Oxide-Based Electronic Synapses for Implementation of Robust High-Accuracy Neuromorphic Computation Systems

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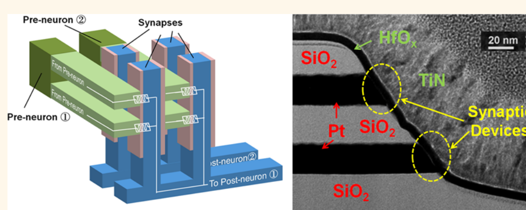
ABSTRACT Neuromorphic computing is an attractive computation paradigm that complements the von Neumann architecture. The salient features of neuromorphic computing are massive parallelism, adaptivity to the complex input information, and tolerance to errors. As one of the most crucial components in a neuromorphic system, the electronic synapse requires high device integration density and low-energy consumption. Oxide-based resistive switching devices have been shown to be a promising candidate to realize the functions of the synapse. However, the intrinsic variation increases significantly with the reduced spike energy due to the reduced number of oxygen vacancies in the conductive filament region. The large resistance variation may degrade the accuracy of neuromorphic computation. In this work, we develop an oxide-based electronic synapse to suppress the degradation caused by the intrinsic resistance variation. The synapse utilizes a three-dimensional vertical structure including several parallel oxide-based resistive switching devices on the same nanopillar. The fabricated three-dimensional electronic synapse exhibits the potential for low fabrication cost, high integration density, and excellent performances, such as low training energy per spike, gradual resistance transition under identical pulse training scheme, and good repeatability. A pattern recognition computation is simulated based on a well-known neuromorphic visual system to quantify the feasibility of the three-dimensional vertical structured synapse for the application of neuromorphic computation systems. The simulation results show significantly improved recognition accuracy from 65 to 90% after introducing the three-dimensional synapses.



KEYWORDS: resistive switching · synaptic device · synapse · metal oxide · memory · 3D integration · neuromorphic computation

Today's computers are characterized by two fundamental attributes: Boolean logic and von Neumann architecture.[1] Despite their tremendous successes, such computers suffer several issues, such as the physical scaling limits of the semiconductor devices and the low efficiency as compared to the biological systems.[2,3] Recently, neuromorphic computing has attracted much attention due to its massive parallelism, adaptivity to the varying and complex input information, and tolerance to fault and error.[4,5] These brain-inspired systems have great potentials for computing with higher efficiency.[6,7] The synapse is a crucial element in biological neural networks.[8,9] Due to the large number of the synapses in a neural network, it is highly desirable to emulate the synapse with a simple device structure that has high density and low-energy consumption.[10−12]

Among the possible candidates, metal-oxide-based resistive switching memory devices have great advantages for the implementation of synaptic devices due to their high performance, low cost, and compatibility with CMOS technology.[6,13] Previous literature has reported that this kind of programmable device has good scalability (less than 10 nm),[14] fast switching speed (about 300 ps),[15] robust cycling endurance (more than 10^{10} cycles),[16] and low operation voltage (less than 2 V).[14,15] Three-dimensional (3D) resistive switching memory array was

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expected to achieve high density integration.[17,18] Furthermore, oxide-based resistive switching devices commonly exhibit multilevel storage ability,[19−21] which could be used as modifiable weights in a neural network.[6] Recently, the spike-time-dependent plasticity and short- and long-term potentiation in resistive switching devices were demonstrated at the device level.[11,22−24]

However, oxide-based synaptic devices need to further reduce the switching current because the energy consumption is one of the key parameters for the electronic synapse application.[25] If the width of the training pulses are around 1 ns, which is the typical clock speed in CMOS circuits, the current of the synaptic device should be substantially less than 10 μA to have energy consumption comparable with the biological one (around 1 to 10 fJ per event).[6] Although the switching current can be controlled by the proper operation scheme,[26] such as applying low compliance current on the device, some negative effects will emerge in this case, which cause the degradation of device performance. One of the most serious problems for resistive-switching-based synaptic devices operated at the low programming current regime is the large resistance fluctuation.[20,26,27] It is widely accepted that the connection and rupture of conductive filaments formed by oxygen vacancies is responsible for the switching phenomenon in the oxide-based resistive switching devices.[28,29] The evolution of the filaments is attributed to the migration of oxygen ions under the electrical and thermal activation. The resistance variation is derived from the random distribution of oxygen vacancies, which is an intrinsic property of the materials. If the device is controlled to work in the low-current regime, the local amount of oxygen vacancies in the filament region becomes less. The reduced number of oxygen vacancies results in the increased variation of the resistance.[30] Although neural networks have strong ability to tolerate errors,[25] the computation accuracy still decreases as the variation in device resistance is increased.[31] The large variation of the synaptic device will seriously block the application of the neuromorphic system.

In this work, we develop an oxide-based synapse with 3D vertical structure. The negative effect from the intrinsic resistance variation can be effectively suppressed on this synapse. The 3D vertical synapse exhibits the potential for low fabrication cost, high integration density, and high efficiency. As an illustration of the use of electronic synapse in a practical system, a pattern recognition application is simulated based on the experimentally measured characteristics of the fabricated devices.

RESULTS AND DISCUSSION

Figure 1a illustrates a typical artificial neural network using a cross-point array of a resistive switching synaptic device at the junction and a CMOS-based neuron circuit at the periphery of the array. The preneuron processes input information and then passes it to the postneuron through synapses. The resistive switching synaptic device changes its conductance under the stimulation of electrical signals. A typical neuron operation involves summation and integration of input signals, with each scaled by the corresponding synaptic weights, and firing occurs if the result exceeds a threshold (Figure 1b).[32] Since each preneuron should be connected to each postneuron through a synapse, the number of synaptic devices is very large. Thus, a 3D array structure with resistive switching device is preferred for providing the high device integration density. For a 3D array, simply stacking the planar array does not save the cost per bit, so a vertical device structure with only one crucial lithography step is a more promising approach.[17] Figure 1c shows the 3D vertical resistive switching device array for synaptic application. The resistive switching synaptic devices are sandwiched between the vertical pillar electrodes and multilayer plane electrodes. The plane electrodes and pillar electrodes are connected to pre- and postneurons, respectively. In this case, the integration density is m times larger than the two-dimensional plane array (m is the number of layers).

As a proof-of-concept work, we fabricated a two-layer resistive switching device array. Pt and TiN are used as plane and pillar electrodes, respectively, while the switching oxide is HfO_x or HfO_x/AlO_y. Figure 1e shows the transmission electron microscopy (TEM) image of the top and bottom cell on the same pillar. Figure 2a shows the typical dc $I-V$ curve of resistive switching process of the fabricated 3D vertical synaptic devices. Both the top and bottom devices show excellent resistive switching behavior with resistance ratio greater than 10^3 and switching voltages less than 3.5 V. The SET (from high resistance state to low resistance state) process is abrupt, while the RESET (from low resistance state to high resistance state) is gradual. Intermediate states, correlated with various length of filament gap, can be controlled by changing the RESET voltage. To reduce the switching current, we apply compliance current on the device during the SET process (Figure 2b). The size of filament can be effectively suppressed by applying a small current compliance, resulting in higher resistance and lower current.

For synaptic training, only slight resistance changes are necessary with each spike. The intermediate states can be modulated by varying the width, the amplitude, or the number of pulses.[21] The last modulation methodology is preferred since it significantly simplifies the design of the programming pulse generation circuit.[25] In this case, a series of identical pulses are applied on the device sequentially. The resistance of the device increases correspondingly as the pulse number increases, as shown in Figure 2c,d. In Figure 2c, the initial

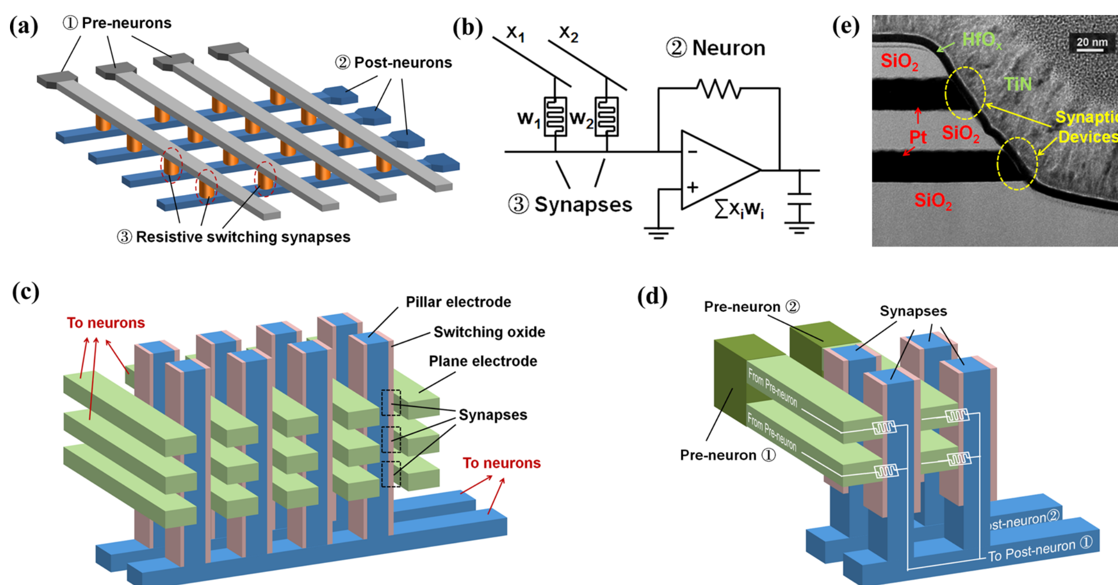

Figure 1. (a) Traditional 2D cross-point array for electronic neural network application. Each top or bottom metal line is connected with a neuron at its terminal. A synaptic device is located at the intersection of each top and bottom metal line. Resistive switching device is one of the choices for the electronic synapse. (b) Implementation of a neuron circuit with resistive switching devices as synapses. The neuron calculates the sum of input weighted by the conductance of synapses and outputs a pulse under some specific conditions. (c) Schematic of the 3D vertical electronic synaptic device architecture for high-density application. Each horizontal or vertical metal line is connected with a neuron. Horizontal lines can be layered many times. An oxide-based synaptic device with a vertical structure is formed at the intersection of each horizontal and vertical metal line. (d) Schematic of the 3D vertical synapse for high-accuracy computation. The vertical metal pillar and all the oxide-based resistive switching devices on this pillar form an electronic synapse. The mean value of these devices reduces the negative effects caused by resistance variation during the synaptic training process. (e) TEM image of the fabricated two-layer 3D vertical oxide-based resistive switching synaptic devices.

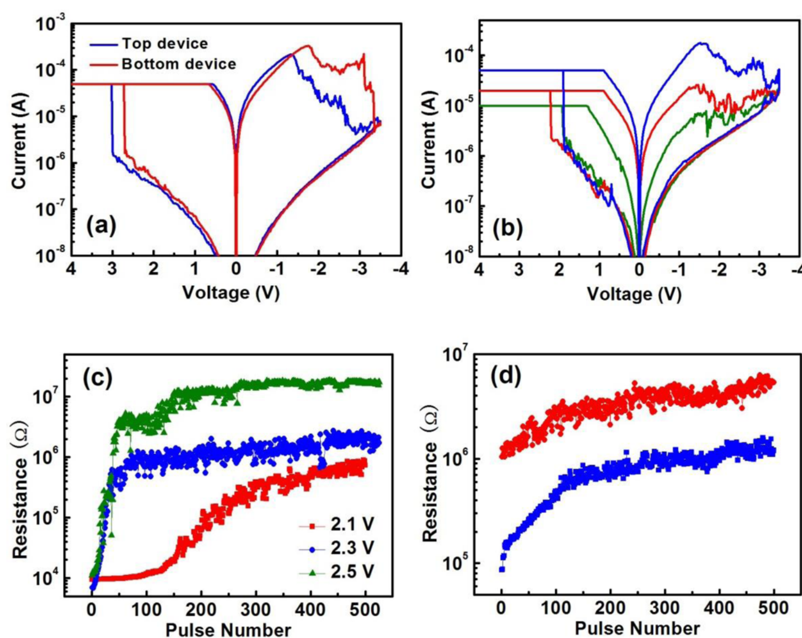

Figure 2. Resistive switching and synaptic training behavior measured on the 3D vertical synaptic array based on the single-cell operation scheme. (a) Typical dc $I-V$ curve of the bipolar resistive switching process measured on the fabricated HfO_x-based 3D vertical synaptic devices. The switching process of top and bottom devices on the same vertical pillar are shown. (b) Resistive switching process with different current compliance. Multilevel switching process is observed. The switching current or energy can be reduced by using small compliance current. (c) Gradual synaptic training process by 500 RESET consecutive identical pulses with different amplitudes. The pulse width is 50 ns. (d) Training process for one device with different initial resistance states achieved by different current compliances during the previous SET cycles. If starting at ~1 MΩ, the maximum energy per spike drops below 1 pJ.

resistance of the device is ∼10 kΩ. After 500 consecutive training pulses (−2.1, −2.3, and −2.5 V per 50 ns) are applied, the resistance gradually increases by more than 100 times and then saturates at a fixed value which increases with the training voltage. The resistance increases and reaches saturation more quickly for larger pulse amplitudes. Smaller voltage leads to more intermediate states, while larger voltage leads to lower total energy consumption in the training process. This phenomenon can be explained by the oxygen migration model: oxygen ions migrate faster under larger electrical field, which increases the speed of oxygen vacancy recombination. The observed voltage dependence of the switching speed is similar to the biological synaptic learning. For example, the stronger stimulus causes quicker study. Since the energy consumption per spike is crucial for synaptic device, to reduce the training energy, we set the initial state of the device to ∼100 kΩ and 1 MΩ by controlling the compliance current in the previous SET cycle. Figure 2d shows the training process that starts from the two initial states. For the initial resistance state of ∼1 MΩ, the maximum energy per spike drops to ∼0.29 pJ. The reduced energy consumption is mainly attributed to the higher initial resistance of the devices. The measurement results demonstrate the feasibility of the 3D resistive switching device array-based synapses for a high-density, low-energy consumption neuromorphic computation system.

Another advantage for the 3D array is to achieve high-accuracy computation. As mentioned above, the resistance variation increases when the synaptic devices are operated in the low-current regime. Normally, we aim to tune the length of tunneling gap between filament tip and electrode to get the gradual resistance change during the training process. During the RESET process, oxygen ions migrate from the cathode to the filament tip, leading to the decreasing length of conductive filament and increasing length of the filament gap region. When the device works in the high-current regime, the amount of oxygen vacancies formed in the conductive filament region is large. For such a thicker conductive filament, the migration of several oxygen vacancies from the filament may not influence the overall resistance of the device (Figure 3a). When the

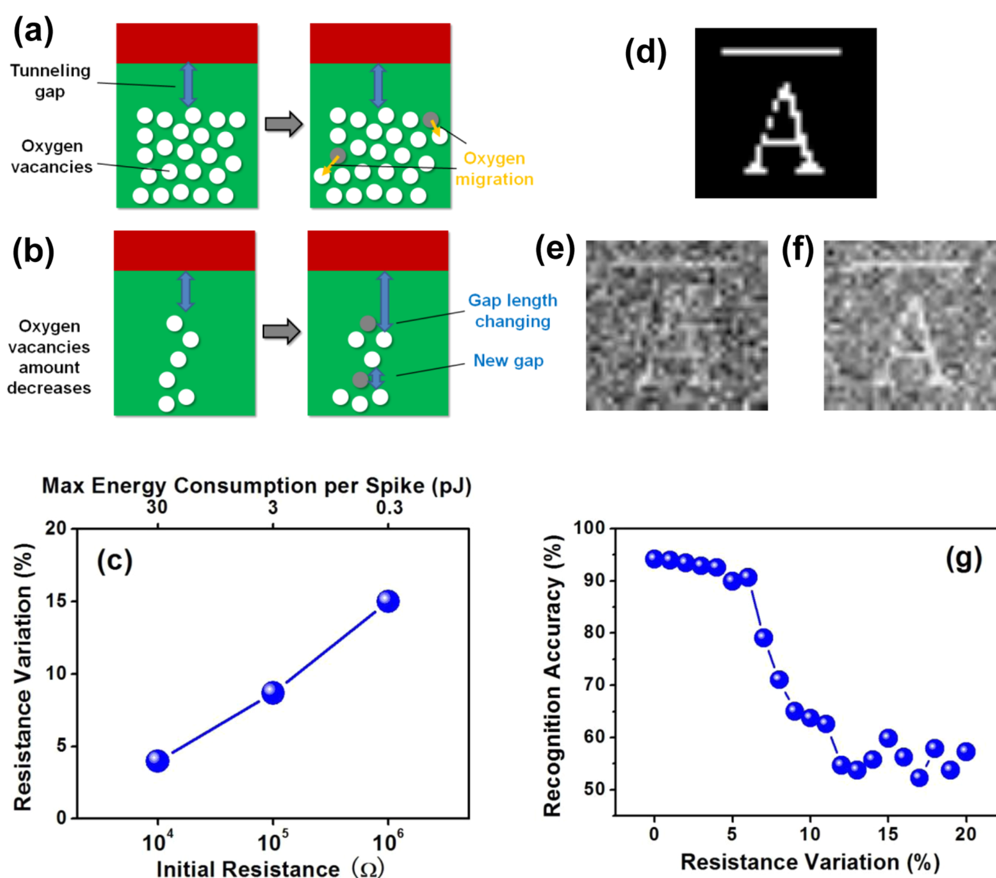

Figure 3. (a) Schematic of the oxygen vacancy conductive filament correlated with high-current regime. (b) Schematic of the oxygen vacancy conductive filament correlated with low-current regime. (c) Extracted resistance variation (based on the data from Figure 2c,d) as a function of energy consumption. (d) Pattern inputted into the neuromorphic visual system for training. (e) Simulated final resistance map of traditional oxide-based resistive switching synapses after training. In the simulation, all the parameters are extracted based on the experimental data shown in Figure 2. Due to the resistance variation of the devices, the system could not be trained very well. (f) Simulated final resistance map of the optimized oxide-based resistive switching synapses using the proposed 3D architecture after training. Compared with panel e, significant improvement could be observed. (g) Simulated accuracy of the system with traditional resistive switching synapses under different device variation.

programming current is smaller, the amount of oxygen vacancies becomes less and the conductive filament is thinner. Some of the key conduction paths may only consist of one or several oxygen vacancies. A small shift of these oxygen vacancies may modify the length of filament gap region or form an additional tunneling gap, which results in an unintentional change of resistance (Figure 3b). Since the migration of oxygen ions due to thermal diffusion and electrical drift is a random process, the resistance variation in the low-current regime is inevitable for resistive switching synaptic devices. To demonstrate this conclusion, we extracted the resistance deviation from the ideal curve, which is fitted based on the measured data in Figure 2c,d. In Figure 3c, it is seen that if the initial resistance is ~10 kΩ, the deviation for the whole training process is less than 5%, while if the initial resistance is ~1 MΩ, the deviation is greater than 15%. It is evident that the pulse-to-pulse variation increases as the initial resistance increases.

To study the influence of resistance variation on the accuracy of the neuromorphic system, a more realistic neuromorphic visual system is built, whose task is to classify the different kinds and orientations of images. The simulated neural network consists of two layers. The first layer contains 32 × 32 input neurons which sense the brightness of a pixel in the source image and convert it into an electrical signal. The second layer contains 16 cortex neurons. All the cortex neurons connect to each input neuron through a 32 × 32 × 16 resistive switching synapses array. In the simulation, hundreds of different images are input for recognition. These images are classified into several categories. Every category is assigned with a specific orientation, and images in it with a different orientation are regarded as recognition failure. Figure 3g shows the recognition accuracy as a function of resistance variation. It can be found that when the initial resistance is 10 kΩ, which corresponds to the variation of 4%, the recognition accuracy is 92.5%. The accuracy drops to 55% when initial resistance is 1 MΩ, which corresponds to the variation of 15%. These results illustrate an important trade-off between the energy consumption and computation accuracy.

One way to solve the fluctuation problem is to use a group of resistive switching devices to mimic a single synapse. The mean value of the devices can effectively suppress the variation. The 3D synaptic array provides a convenient structure to connect in parallel multiple devices at the intersection of each lines connected to the pre- and postneurons. As illustrated in Figure 1d, the resistive switching devices on different layers with the same pillar can be viewed as a synaptic device. These devices receive the same training pulses at the same time. Figure 4a shows the measured training process based on such an operation scheme. Two devices on the same pillar are trained and read at the same time. The gradual resistance changes observed on both of the devices indicate that there is no interference during the training or readout process.

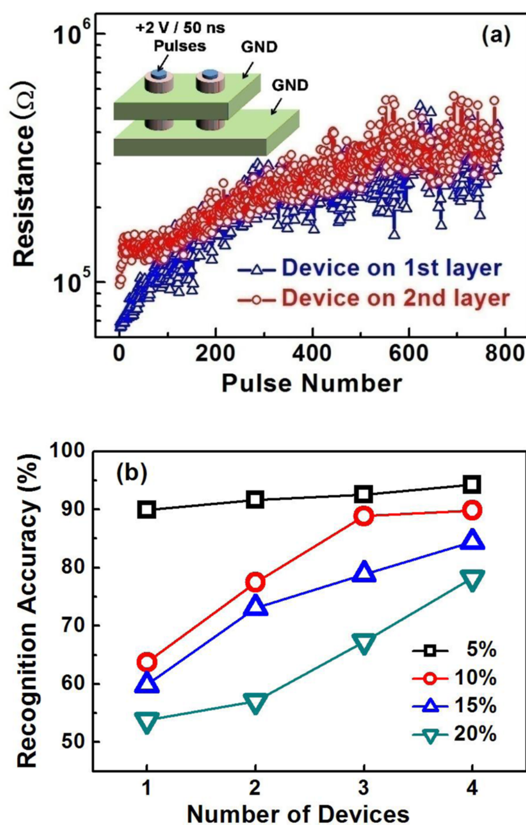

Figure 4. (a) Training process for the synapse consisted of two resistive switching devices. Inset: schematic of measurement setup. The two devices sharing a same vertical metal pillar are trained at the same time. In the training process, voltage pulse is applied on the pillar electrode, while the two plane electrodes are grounded. (b) Simulated pattern recognition accuracy as a function of resistance variation. The synapses consisting of different number of oxide-based resistive switching devices are shown.

To evaluate the degree of accuracy improvement of such methodology, we simulate the pattern recognition process based on the performance of the 3D array. It is found the resistance variations extracted from the top device and bottom device are 9.8 and 7.5%, which results in a ~65 and ~70% recognition accuracy if using a single device as synapse (Figure 3e). After combining the two devices as a synapse, the variation of the mean value is ~5.9%, which corresponds to a recognition accuracy of 90%. Significant improvement on resistance uniformity of devices and recognition accuracy of the system is achieved by using the 3D synapses. Adding more resistive switching devices on one synapse is expected to get a better accuracy. Figure 4b shows the simulation results of the recognition accuracy as a function of device number and resistance variation. A signification improvement is observed when using more devices in parallel as a synapse. This methodology can be achieved by adding more layers on the 3D array. Based on the structure

shown in Figure 1d, the number of the resistive switching devices for one synapse is dependent on the layers of plane electrode, adding which moderately increases the fabrication cost. The density of the synapses implemented in this structure is still $4F^2$ (F is the feature size of the fabrication technology), which is similar to the 2D cross-point architecture.[28] It should be noticed that with more devices stacked in parallel, the recognition accuracy is improved significantly, while the energy consumption increases linearly with the stacked device number. Therefore, to keep the same recognition accuracy, the 3D synapse with low current can achieve much lower energy consumption than single device with high current.

CONCLUSION

To summarize, we experimentally demonstrated 3D vertical resistive switching electronic synaptic devices. Low training current (<3 μA), gradual resistance transition with hundreds of intermediate states, fast speed (50 ns), low training voltage (<2.5 V), and robust device-to-device repeatability are measured. A training operation scheme on the 3D synapses is proposed by combining several devices on the same vertical pillar as a single synapse. The negative effects caused by resistance variation, which is intrinsic to the resistive switching synaptic devices, can be effectively suppressed based on the novel scheme. A pattern recognition computation is simulated based on the established neuromorphic visual system to quantify the variation effects. The simulation result shows significant improvement of recognition accuracy after using the novel training scheme on the proposed 3D neuromorphic computation system.

METHODS

Device Fabrication. We develop an oxide-based synapse with 3D vertical structure. The schematic of the process flow is shown in Supporting Information S1: First, multilayer stacked Pt (22 nm) and SiO_2 (33 nm) are deposited by e-beam evaporation and plasma-enhanced chemical vapor deposition, respectively. Next, a trench (1−100 μm in size) is dry etched down to the bottom SiO_2 layer to form the active memory region. Then HfO_x layer of 5 nm or AlO_y/HfO_x layers of 3 nm/3 nm are deposited by atomic layer deposition successively, which conformally covers the sidewall of the trench. Then, 150 nm TiN is deposited by reactive sputtering to fill the trench as the pillar electrode. Finally, contact vias to the Pt plane electrode are formed by dry etching so it can be separately contacted electrically. The synaptic devices are formed at the sidewall between the TiN pillar electrode and Pt plane electrode with two cells on the sidewall per trench.

Electrical Measurements. Direct current measurements are performed using the Agilent B1500A semiconductor device parameter analyzer combined with a probe station (Cascade). In the measurement, voltage is applied on the plane electrode (Pt), while the pillar electrode (TiN) is grounded. Current compliance is applied to protect the device and to control the filament size. Pulse measurements are performed using a combination of Agilent B1500A semiconductor device parameter analyzer, Agilent 33250 function/arbitrary waveform generator, and a switching matrix. Resistance is read using dc method after each pulse is applied.

For the single-cell operation, a half voltage program scheme is adopted to avoid unintentionally writing on the unselected cell. SET or RESET voltage is applied on the selected plane electrode, while another voltage, which equals the half value of the SET or RESET voltage, is applied on the unselected plane electrode. Therefore, only the selected cells will see a full write voltage, while unselected cells will see a half write voltage. For the array read operation, the unselected plane electrode is grounded to avoid the misreading caused by the sneak path effect.

For the synaptic operation, SET or RESET is performed at the same time on the devices sharing the same pillar electrode. In this case, SET or RESET voltage is applied on the vertical pillar electrode, and the plane electrodes are grounded. In the SET process, current compliance is applied on all the plane electrodes, while the pillar electrode does not receive current compliance.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Details on device fabrication, forming process, uniformity, simulation on oxygen vacancy distribution evolution during synaptic training process, methodology to extract the resistance variation, and simulation method for the neuromorphic system. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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